A High-Performance GaAs SP3T Switch for Digital Cellular Systems

Zeji Gu, Shuyun Zhang, David Johnson, Steve Belletete, Mark Ayvazian, and Dave Fryklund

Alpha Industries, Inc., 20 Sylvan Road, Woburn, MA 01801

***Abstract*: A high-performance GaAs SP3T switch has been developed using asymmetrical design of the transmit and receive paths. A combination of stacked FETs and multi-gate PHEMT FETs with high breakdown voltages and large peripheries was implemented in this design. Insertion loss of less than 0.8 dB and isolation greater than 25 dB to 2 GHz were obtained. With a positive 3-V control voltage, power handling of the device exceeded 34dBm while maintaining second and third harmonic levels better than 65dBc.**

I. INTRODUCTION

Recent popularization of digital cellular systems has accelerated the GaAs switch technologies. Since most digital cellular systems have adopted TDMA communication, a T/R antenna switch connecting an antenna to a transmitting circuit (Tx) or receiving circuit (Rx) is indispensable in these systems. Some critical performance parameters needed in the T/R antenna switch are high linearity, high power handling, low insertion loss and high isolation. The development of GaAs MMIC switches is desired since FET switches have the advantages of low power consumption, high switching speed, and simplified bias networks when compared to diode switches that require continuously applied bias currents for operation. Furthermore, there is a need to change the control voltage of the FET switch to 0/+3V from the conventional voltage of 0/-5V.

Although many power GaAs MMIC switches have been developed [1]-[3], these switches cannot be operated at low control voltages and still maintain high power handling, high linearity, low insertion loss and high isolation.

In this paper, we describe a new SP3T GaAs PHEMT switch which achieves high performance by using asymmetrical design of the transmit and receive paths and a combination of stacked FETs and multi-gate PHEMT FETs with high break-down voltage and large peripheries. We have also implemented a novel idea to improve isolation by using capacitors for series resonance in the shunt circuit of the receiving side of the switch.

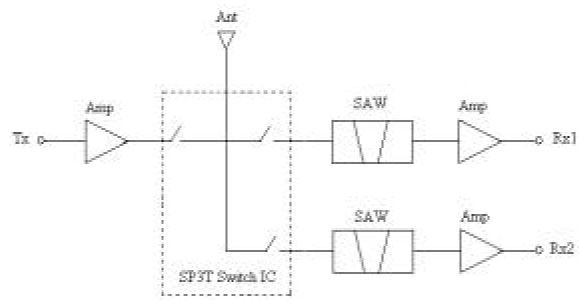

Fig. 1. Configuration of SP3TAntenna Switch

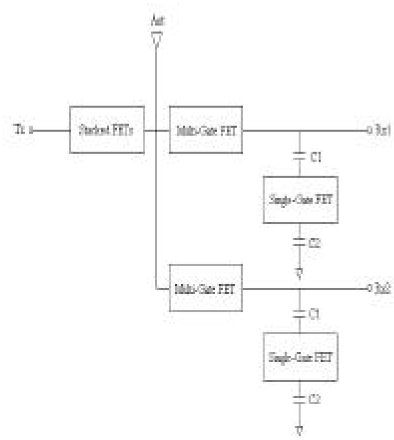

Fig.2. Configuration of SP3T Switch IC

II. CIRCUIT DESIGN

Fig. 1. Shows the configuration of SP3T antenna switch. The SP3T switch IC is described in Fig. 2. Since the RF output power from a power amplifier in cellular handset is usually high and the loss in the antenna switch causes the increase in output power from the power amplifier and the decrease of the available usage time. Therefore, a high-power switch with low insertion loss,

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high isolation and high linearity is desired for use in a cellular phone.

A. FET Switch Power-Handling Capacity

At RF frequencies, the maximum power handling of a FET switch is determined by its voltage swing in the off state and drain current density in the on state. By increasing the breakdown voltage of the individual FETs or by increasing the number of stacked FETs, the maximum voltage swing may be increased. The RF breakdown voltage may be improved by implementing a series chain of single gate FETs used as capacitive voltage dividers. A resulting problem is that the series combination increases insertion loss. However, if the on resistance for the individual FETs is small enough, as is the case for the PHEMT FETs, the total resistance for three stacked FETs is acceptable.

The current handling capability of a FET can be increased in proportion to its periphery. A major problem with increasing periphery is the resulting increase in the off state capacitance, which provides a low isolation in the transmit side and a high insertion loss in the receive side of the switch.

Recently a multi-gate approach has been used to improve power handling. This structure exhibits improved insertion loss over the series FET combination. It has been reported [1] that the power handling is at least equivalent to and potentially better than the series FET combination. The use of the multi-gate FET in place of a stack of individual FETs reduces device area with a resulting reduction of parasitic inductance and capacitance, and the voltage is split more evenly in the multi-gate FET than that in the multi-FET line up, therefore, power handling is somewhat higher.

The antenna switch IC for cellular phone applications has to be capable of transmitting at least 30dBm of power with little distortion. When receiving, however, the power level of the signal is very low because of propagation through the air. This power can be as low as 0dBm. It is only necessary to operate at a relatively high power level when the IC is being used as an antenna switch in the transmit mode. Based on the above consideration, we adopted a circuit configuration that incorporates three series FETs in the transmit side and a triple-gate FET in series with a shunt single FET in the receive side. Fig. 2 shows the circuit configuration.

B. Low Insertion Loss/High Isolation

The key for a successful design that achieves the required switching characteristics is the reduction of on-state resistance (Ron) and off-state capacitance (Coff). Shortening the recess length and increasing the sheet electron density can decrease the on-resistance, which is mostly determined by the channel resistance beneath the gate. PHEMT has a higher sheet electron concentration compared with other GaAs FETs, such as MESFET, so is a good choice for a low Ron and low insertion loss. On the other hand, shortening the recess length and making the electron density higher results in a higher Coff, which decreases isolation. This relationship is widely acknowledged to be a trade-off situation. It appears to be very difficult to develop high performance FETs that satisfy both low Ron and low Coff. However, by utilizing resonance characteristics, it is possible to obtain high isolation while maintaining low insertion loss, allowing us to design the switch IC without considering the trade-off between insertion loss and isolation.

The design of a conventional resonant-type switch IC [4] is accomplished by placing a monolithically fabricated inductor in parallel with the source-drain region of each series FET to generate a parallel-LC resonator. We propose a new resonant-type switch IC that places a capacitor in series with the shunt FET to create a series-LC resonator at the receiver side of the switch. As shown in Fig. 2, the receiver side is composed of a triple-gate FET with a single gate FET in shunt. The bonding wire is used as the inductor, with resulting values of 0.8 – 1.0nH. Through deliberate design we produce series LC resonance, and the corresponding resistance exists during the on state of the shunt FET. While in the on state, the FET can be simplified by a series resistance Ron [5]. High isolation exists at the frequency approximated by $1/(2p)\sqrt{\frac{C_1+C_2}{C_1C_2}}$ for 1nH inductance. By choosing different values of C_1 and C_2, the high isolation of the design can be achieved. Furthermore, if C_1 is on chip and fixed, C_2 can be adjusted externally to meet the isolation requirements at specific frequencies.

III. PERFORMANCE

Measurements have been performed at room temperature on ten plastic parts.

The PHEMT FETs used in this design have gate widths of 200um for each series FET in the transmit side, 200um for the series triple-gate FET, and 100 um for the shunt single gate FET. All gates have the same length of 0.5um and 10 fingers. The shunt fixed capacitor is 11pF, and the resistance applied to each gate is 10 $k\Omega$. The chip size is 0.85 mm $\times$ 0.96 mm. Fig. 3 shows the top view of the plastic part of the SP3T antenna switch.

Fig. 4 shows the measured relationship between isolation and frequency. The relationship of resonant frequency as a function of capacitance can be seen more clearly as shown in Fig. 5. The various isolations have been measured: Rx2 isolation when Rx1 is in the on-state, Rx1 isolation when Tx is in the on-state and Rx1 isolation when Rx2 is in the on state. Below 1 GHz, high isolation is only available if C_1 is increased. For a fixed value of C_1 (11pF), a high value of capacitance for C_2 has little effect on the series LC resonance. The resonant frequency remains nearly constant, and is mostly dependent on C_1.

Fig. 6 shows the measured large-signal characteristics of the device's insertion loss and isolation at power inputs of 32dBm and 34dBm. Insertion loss of 0.8 dB and isolation of 32 dB at 2 GHz was achieved in the transmit mode. The isolation was about 6dB lower at 2 GHz than at 1GHz, which shows the effectiveness of the novel resonant-type shunt circuit. The device has impressive high power operation with low distortion even while operating at the low control voltage of 0/3 V. The harmonic content of the output with 32dBm and 34dBm input power is shown in Fig. 7 and Fig. 8. All harmonics are approximately 70dB below the fundamental.

IV. CONCLUSION

Compared with previously reported designs, our newly developed high linearity SP3T MMIC switch is capable of high power handling and high isolation at low control voltages. This was achieved with the novel resonant-type shunt FET circuit.

ACKNOWLEDGEMENT

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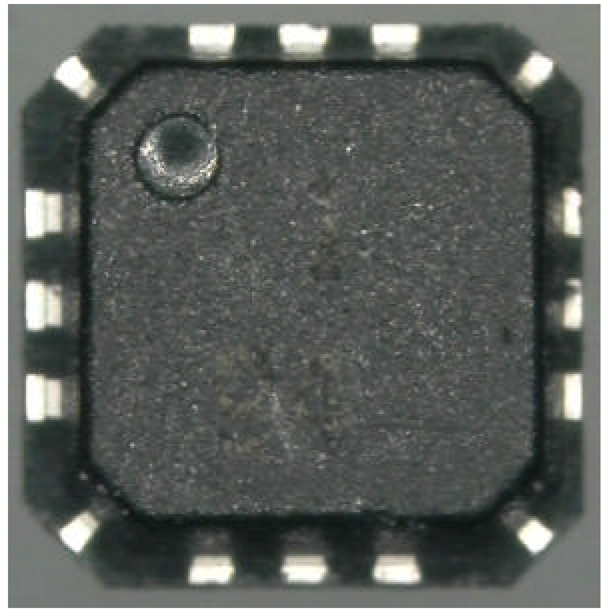

Fig. 3. SP3T antenna switch with a MLP-12 lead plastic package with size: $3mm \times 3mm$.

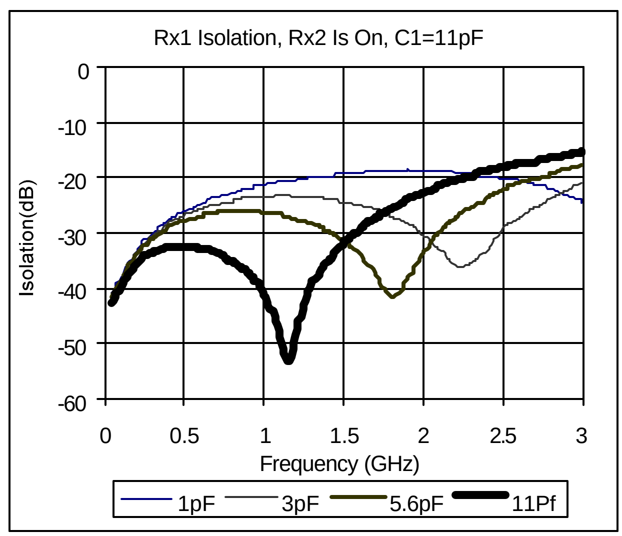

Fig. 4. Rx1 isolation as a function of frequency for various C2 values.

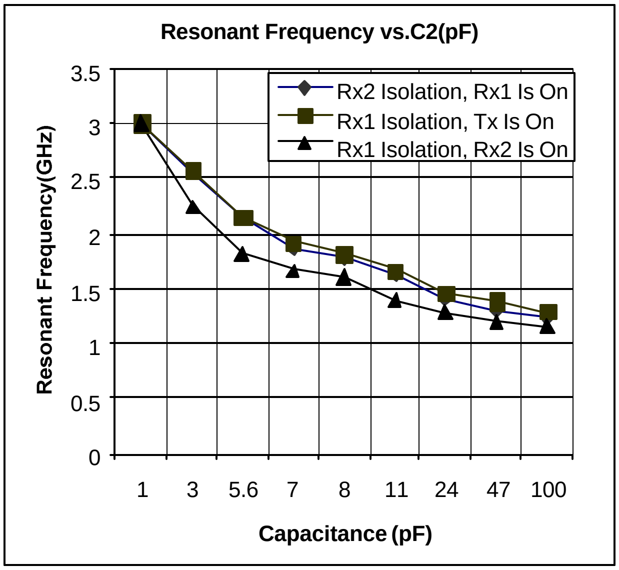

Fig. 5. Resonant frequency as a function of capacitance.

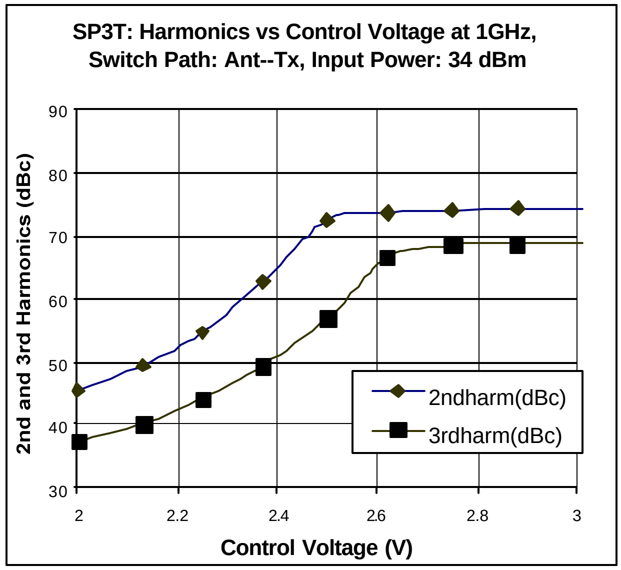

Fig. 7. Distortion characteristics as a function of control voltage.

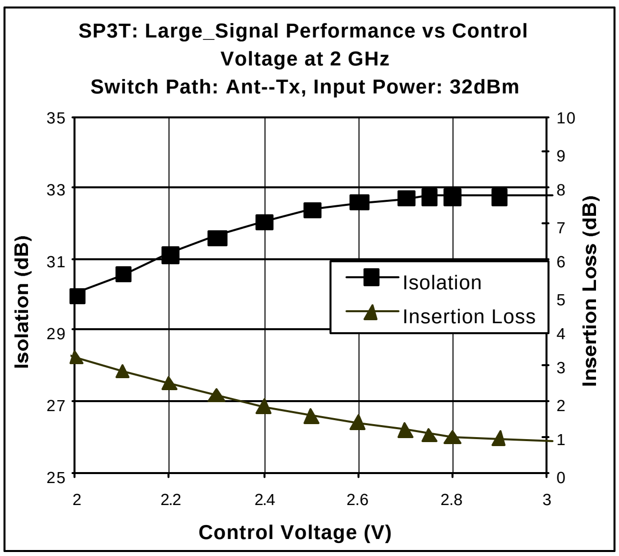

Fig. 6 Insertion loss and isolation as a function of control voltage.

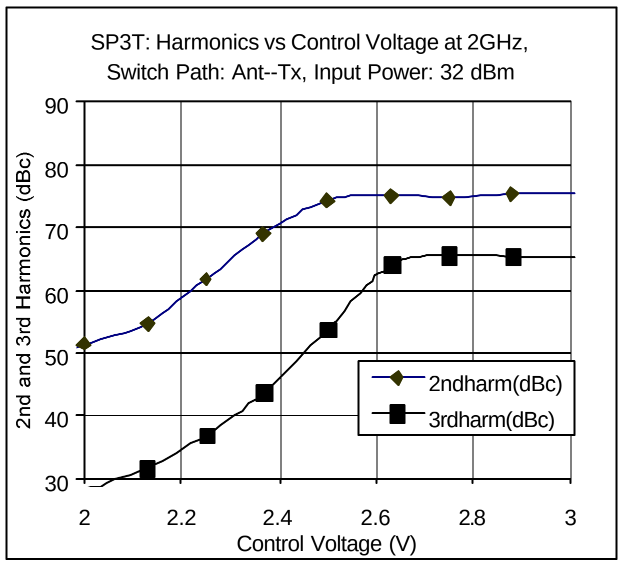

Fig. 8. Distortion characteristics as a function of control voltage.